ALEXANDRE VALENTIN JAMET

PhD Candidate – Computer Science / Computer Architecture

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@jesuisalexjamet | 0000-0001-6119-0213 | +34 640 306 376

PROFESSIONAL GOALS

PhD in Computer Architecture with a Master's degree in Embedded Software. Specialized in optimizing CPU data movement and performance. Extensive experience working across research labs, industry partners, and cross-disciplinary teams to address memory bottlenecks and enhance virtual memory systems. Skilled in leveraging AI-driven techniques to improve system efficiency, with a strong ability to translate complex technical insights into actionable strategies for diverse stakeholders. Looking for an exciting new challenge.

WORK EXPERIENCES

Researcher – Computer Architecture

Barcelona Supercomputing Center

October 2018 – Ongoing | Barcelona, Spain

- Carrying research in the *Runtime Aware Computer Architecture* group in the Barcelona Supercomputing Center on the interaction between Computer Architecture and Artificial Intelligence.
- Published multiple research papers in top-tier international conferences in Computer architecture.
  - ***Practically Tackling Memory Bottlenecks of Graph-Processing Workloads***.
    Published in IPDPS'24. Presents a micro-architectural development of the cache hierarchy that separates regular and irregular memory accesses.
  - ***A Two Level Neural Approach Combining Off-Chip Prediction with Adaptive Prefetch Filtering***.
    Published in HPCA'24. This paper leverages off-chip prediction for adaptive prefetch filtering.
  - ***Characterizing the Impact of Last-Level Cache Replacement Policies on Big-Data Workloads***.
    Published in IISWC'20. This paper exposes the ineffectiveness of classic cache management schemes.

Intern – Feasibility Study of a Maritime Routing System

D-ICE ENGINEERING

June 2018 – October 2018 | Nantes, France

- Integrated a maritime routing suite into a test-bed sailing boat throughout an internship at D-ICE ENGINEERING.
- Analyzed data consumption of the tool, identified shortcomings in the company's business model related to weather prediction.
- Based on the outcome of the proposed model, I suggested solutions to provide the company's clients with a viable solution through a cloud-based approach.

Industrial Project – PoC of a GSM-LoRa Gateway

French Ministry of Armed Forces

October 2017 – March 2018 | Paris, France

- Developed a PoC of a GSM to LoRa Gateway for the French Army.
- Prototype created on an ARM Cortex-M0 chip with FreeRTOS.
- The prototype was proven able to receive text messages and transfer them over a distance of 1.5 km using the LoRa protocol.

ACHIEVEMENTS

Sport
Participated in the 2018 Finswimming World Championships.

Non-profit Organization
Raised lottery funds for finswimming equipment and international competition trips.

TECHNICAL SKILLS

Performance Engineering | C/C++ | Computer Architecture | Assembly | Shell | Python | VHDL | OpenMP | Jupyter Notebooks | GDB/LLDB | Clang Stack

LANGUAGES

French
English
Spanish

EDUCATION

PhD Candidate

Barcelona Supercomputer Center / Universitat Politecnica de Catalunya

2018 – 2024 | Barcelona, Spain

- Worked on developing predictors leveraging AI-inspired methods.
- Published research papers in top-tier international conferences on Computer Architecture: IPDPS, HPCA, and IISWC.

Graduate School of Engineering

TELECOM Nancy, France

2015 – 2018 | Nancy, France

- Major in Computer Sciences, minor in Embedded Software.
- Focus on Computer Architecture.

Preparatory Classes to Graduate Schools

LGT Baimbridge, Guadeloupe

2013 – 2015 | Les Abymes, Guadeloupe

- Major subjects: mathematics, physics, and chemistry.

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PUBLICATIONS

- **A. V. Jamet, G. Vavouliotis, L. Alvarez, D. A. Jiménez and M. Casas**, *"Practically Tackling Memory Bottlenecks of Graph-Processing Workloads"*. To appear in the 38th IEEE International Parallel & Distributed Processing Symposium (IPDPS), May 2024.
  - **Paper**: 10.1109/IPDPS57955.2024.00096
  - **Slides**: 10.5281/zenodo.11398316.
- **A. V. Jamet, G. Vavouliotis, L. Alvarez, D. A. Jiménez and M. Casas**, *"A Two Level Neural Approach Combining Off-Chip Prediction with Adaptive Prefetch Filtering,"* 2024 IEEE International Symposium on High-Performance Computer Architecture (HPCA), Edinburgh, United Kingdom, 2024, pp. 528-542, doi:
  - **Paper**: 10.1109/HPCA57654.2024.00046
  - **Slides**: 10.5281/zenodo.10789477.
  - **Poster**: 10.5281/zenodo.10797183.
  - **Artifact**: 10.5281/zenodo.10113336.
- **A. V. Jamet, L. Alvarez, D. A. Jiménez and M. Casas**, *"Characterizing the Impact of Last-Level Cache Replacement Policies on Big-Data Workloads,"* 2020 IEEE International Symposium on Workload Characterization (IISWC), Beijing, China, 2020, pp. 134-144, doi:
  - **Paper**: 10.1109/IISWC50251.2020.00022.
  - **Presentation**: Watch the presentation on YouTube.
  - **Slides**: 10.5281/zenodo.10563544.

WORKSHOPS

- **A. V. Jamet, L. Alvarez and M. Casas**, *"Characterizing the impact of last-level cache replacement policies on big-data workloads"*. 10th Barcelona Supercomputing Center Doctoral Symposium, May 2023. doi:
  - **Extended Abstract**: 10.48550/arXiv.2305.06696.

PATENTS

- **European Patent Application EP 4575807 A1** — "Perceptron-Based Off-Chip Predictor" Inventors: A. V. Jamet, G. Vavouliotis, M. Casas. Filed Dec 2023, published Jun 2025.

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